[0038] ABSTRACT

[0039] A packet processing system converts a wide bus carrying P packets to a narrower bus that can carry only Q packets, where $Q < P$. The packet processing system includes a first data path, a queue, a shift register and a control unit. The first data path receives up to P packets during a first processing cycle. The queue stores the P packets in a queue. The control unit shifts a first quantity of data of the P packets into the shift register from the queue and selectively retrieves data from the shift register until a first packet of the plurality of packets is retrieved. The control unit then sends the first packet on a second data path during the first processing cycle.